Purpose: Minimize inter-chip or inter-circuit coupling through the power ports. This includes two ports: power and ground.

BYPASSING

Digital circuits primarily cause fast transient changes in $i_t$. This occurs with CMOS, for example, when significant current is drawn only during switching.

$Q_1$, $Q_2$ pass through the 3 usual states when $V_i$ changes logic levels:

- $V_i = 0 \Rightarrow V_o = V_{DD}$, $Q_1$ triode, $Q_2$ cutoff, $i_t = 0$
- $V_i = \frac{V_{DD}}{2} \Rightarrow V_o = \frac{V_{DD}}{2}$, $Q_1$ SAT, $Q_2$ SAT, $i_t$ is maximum
- $V_i = V_{DD} \Rightarrow V_o = 0$, $Q_1$ cutoff, $Q_2$ triode, $i_t = 0$
The Problem: 

Visit changes during the current spike due to \( L_{wp} \) and \( L_{wr} \), i.e., 

\[
V_{wave} = L_w \frac{di}{dt} = L_w \frac{di'}{dt}
\]

In order to have an idea of magnitudes involved, consider a 74HC04 inverter:

![Diagram of a 74HC04 inverter circuit]

It may switch in 10 ns and draw a peak current of 50 mA, let \( L_{wp} = 100 \text{ nH} \).

\[
\frac{\Delta i}{\Delta t} = \frac{\Delta I}{\Delta t} = \frac{50 \text{ mA}}{10 \text{ ns}} = 500 \text{ mA/} \mu \text{s}
\]

let \( L_{wp} = L_{wr} = 200 \text{ nH} = L_w \)

\[
\Delta V_{wo} = \pm L_w \frac{\Delta i}{\Delta t/2} = \pm 200 \text{ nH} \times \frac{500 \text{ mA}}{5 \times \text{ns}} = \pm 2 \text{ V}
\]

\( V_{chp} \) will not be stable at 5 V!

You can easily see this spike-like waveform at the power pins (a, b) of digital chips.

Placing a "bypass capacitor" directly across pins a and b will greatly decrease \( \Delta V_{chp} \).
worry that $\frac{\Delta V_c}{V_c} \Rightarrow \Delta V_c \approx \frac{\Delta V}{C}$

\[ \Delta V_c \]

\begin{align*}
100 \mu F & \quad 5 \text{ [V]} \\
1 \mu F & \quad 0.5 \text{ [V]} \\
10 \mu F & \quad 50 \text{ [mV]} \\
100 \mu F & \quad 5 \text{ [mV]} 
\end{align*}

"Rule of Thumb" value for most digital circuits.

Regardless of the varying inductance, the capacitor will stabilize $V_c$ to less than 5 mV during current transients.

The practical action is actually more complicated since $L_w$ and $L_w$ and bypass form a parasitic series resonant circuit:

\[ \frac{1}{2 \pi \sqrt{L_w C_{\text{bypass}}}} \quad \eta_0 = \frac{V_c}{R_T} = \left| \frac{j \omega L_w + \frac{1}{C_{\text{bypass}}}}{R_T} \right| \]

If the power supply is very good, $R_T \rightarrow 0$, but $R_{\text{chip}}$ is usually small enough to influence the effective loaded $\eta_0$.

AC model:

\[ \frac{1}{s L_w} \quad \frac{1}{C_{\text{bypass}}} \]
RF circuits primarily need interstage isolation more than current transient stability since supply currents don't change digitally, but are more sinusoidal.

**Basic Idea:** Lower inter-stage coupling through the power supply parts by

1) Filtering with low Q's.
2) Carefully pay attention to where parasitic resonances may occur.

Therefore, techniques vary depending on isolation requirements.

a) RFC ("Radio Frequency Choke")

\[ \frac{L_C}{R_C} \]

Add \( R_C \) to lower \( Q \)

\( L_C \) is very high to effectively block or "choke" RF sinusoids.

b) Provide axial frequency range bypassing.

Since caps are not I0SAIC:

\[ \frac{100\mu F}{10\mu F} \]...\[ \frac{100\mu F}{10\mu F} \]

Excellent low reactance to high frequencies

Excellent low reactance to lower frequencies that \( C \) is ineffective at.

Choose capacitors based on where the SRF points fall.